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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,541	04/18/2001	Ryan C. Kinter	1778.0200000	6813

26111 7590 07/16/2009

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	
MAIL DATE	DELIVERY MODE
07/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/836,541	KINTER ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8,10-14 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5,6,8,10-14 and 30-32* is/are allowed.

6)☒ Claim(s) *21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of the following is required (Claim 10 is reciting computer program product. However no clear and deliberate definition of computer program product can be found in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-23, 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Brennan (patent No. 5,740,392).

As to claim 21,27, Brennan taught the invention substantially as claimed including decoding instructions in a processor comprising (a)mapping each of a plurality of instructions to a predetermined instruction width forma (PIWF) configuration (see length 00H and 0FH as the format configuration in fig. 5); (b) comparing in parallel with (a), tag for each of said plurality of instructions to an address (see detection of most significant bits with 0FH in col. 6, lines 40-52, most significant bits 0-2); (c) selecting, based on the comparison in the comparing, one of the PIWF configurations of the

configuration to be decoded (see select signal [select]) and (d) decoding PIWF configuration selected for execution by processor core (see fig. 5 decoders, see also the length decoders 40 and 35 in col. 6, lines 66-67, col. 7,lines 1-49, see also parallel decoders in fig. 8).

As to the limitation in claim 21 wherein each tag is associated with a single instruction the limitation is does not restrict the number of instructions associated with a tag but only requires a single instruction to be associated with the tag. Brennan taught the association of a tag with at least a single instruction (e.g., see col. 6, lines 15-33).

As to claims 22,23,25,26, Brennan also included 16 bit and 32 bit (see fig. 2, Prefix (1-15) and 32 Bits).

Claim Rejections - 35 USC § 103

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) in view of Overkamp.

As to claim 28 Brennan taught a processor comprising a) mean for mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration (see configuration (see length 00H and 0FH); and c) multiplexer for receiving the PIWF configurations from means for mapping and for selecting, in response to a selector signal [select], desired one of the PIWF configurations for decoding and execution by the processor (see also the length decoders 40 in 35 col. 6, lines 66-67, col. 7,lines 1-49, see also a plurality of parallel decoders in fig. 8, see the shifter 38 used as a mux in col. 6, lines 40-52) (e.g., see col. 6, lines 15-33).

As to claim 28, Brennan taught mapping maps an instruction to a PIWF configuration (e.g., see col. 5, lines 3-24)(also see the length decoders 40 in 35 in col. 6, lines 66-67, col. 7,lines 1-49, see also a plurality of parallel decoders in fig. 8, see the shifter 38 used as a mux in col. 6, lines 40-52).

Brennan did not expressly detail a decoder decoding the desired one of said PIWF configurations for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction configuration selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Claims 24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) in view of Lee (patent No. 6,442,674).

As to the limitations of claims 24, limitations of claim 21 have been discussed in previous paragraph.

Brennan did not specifically show a fill buffer as claimed. Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed

because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a movtivation. Also the incorporation of the Lee teachings would have yielded predictable results.

Claims 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (patent No. 5,740,392) and Overkamp patent No. 7,069,420) in view of Lee (patent No. 6,442,674).

As to the limitations of claims 29, limitations of claim 28 have been discussed in previous paragraph.

Brennan did not expressly detail a decoder decoding the selected mapped instruction for execution by the processor. Overkamp however taught this limitation (e.g., see fig. 5 decoder 535 decodes the desired instruction selected via the 64 bit and 2 bit multiplexers (e.g., see col. 3, line 5-col. 4, line 63).

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Brennan and Overkamp. Both references were directed toward the problems of decoding instruction of different width in data processor. One of ordinary skill would have been motivated to incorporate the Overkamp teaching of decoding the

selected instruction with an indicated instruction with at least to facilitate the decoding of decoding of instructions of different widths from multiple sources. Also the incorporation of the Overkamp teachings would have yielded predictable results.

Brennan did not specifically show a fill buffer as claimed. Overkamp taught a loop buffer which would have provided a filling operation of loop instructions when a loop was been executed (e.g., see fig. 5). On the other hand Lee taught a fill buffer (see fig. 1 [100], col. 2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g., a buffer, or the like), therefore the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see, fig. 4) [instruction cache 30], which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have bee provided in the system to increase the read/write speed of the instructions, and in doing so, provided a movtivation. Also the incorporation of the Lee teachings would have yielded predictable results.

Allowable Subject Matter

Claims 1-3, 5, 6, 8, 10-14, and 30-32 are allowed.

Response to Arguments

Applicant's arguments filed 5/6/09 with have been fully considered but respect to claims 21-29 they are not persuasive.

Applicant argues in substance that the 35 U.S. C. 101 should be withdrawn with the inclusion of the "computer readable storage medium" language in claim 10 and in claim 30. The 35 U.S. C. 101 rejection of Claims 10-14 and 30 has been withdrawn.

Applicant argues as to claim 21 the language wherein each tag is associated with a single instruction and comparing each tag to an address. The Examiner contends that Brennan shows in the addressing of a page the comparing of a tag with a page address (e.g., see col. 6, lines 15-33). Also as to the argument regarding the single instruction address associated with each tag that is discussed in the outstanding rejection above.

As to the argument that in claim 31 that the parallel mapper is upstream, Brennan taught the upstream mapping of instructions in the fetch stage (e.g, see col. 6, lines 15-33 however with the other limitations of claim 31 in combination with the limitations of the parallel mapping, tag comparison and selection are completed in a single pipeline stage, this combination is not deemed to be taught by Brennan and therefore claim 31 is not now rejected.

As to the arguments pertaining to claims 1-3,5,6,8,10-14,30-32, the arguments were persuasive and claims 1-3,5,6,8,10-14 and 30-32 are not now rejected under 35 U.S.C. 102 or 35 U.S.C. 103.

Applicant argues that claim 28 recites multiplexor for receiving PIWF configurations from said mapper and for selecting a selector signal, a desired one of said configurations for decoding and execution by the processor. Examiner contends that the mapper in the fetch stage send plural configurations to the decode stage that is that are input in parallel to a corresponding multiplexor for selection of the in response

to a selection signal (e.g., see figs . 4, 5 and col. 5, lines 3-24 col. 6, lines 15-33 and outstanding rejection above). As claims 24 and 29 are argued as having the limitations of claim 28 the Examiners response to claim 28 applies to claims 24 and 29)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

/Eric Coleman/
Primary Examiner, Art Unit 2183